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CLAIMS

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What is claimed is:

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1. Structure comprising:

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a printed circuit board containing a plurality of component contacts for receipt of electronic components;

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a plurality of electrically conductive traces formed on said printed circuit board, each trace being electrically connected to a corresponding one of said component contacts; and

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at least one integrated circuit mounted on a selected portion of said printed circuit board and containing a plurality of conductive leads, each of said conductive leads being electrically connected to a corresponding one of said electrically conductive traces formed on said printed circuit board thereby to form an electrically conductive path from each of said conductive contacts to the corresponding conductive leads on said at least one integrated circuit, said at least one integrated circuit being configurable by a user to interconnect selected electrically conductive traces on said printed circuit board to achieve a desired electrical function from the electronic components to be connected to said printed circuit board.

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2. Structure as in Claim 1 wherein said printed circuit board contains more than one layer of conductive traces.

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3. Structure as in Claim 1 wherein at least some of said plurality of electrical contacts comprise a plurality of holes in said printed circuit board, each hole being appropriate for receipt of a conductive lead of an electronic component.

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4. Structure as in Claim 3 wherein the interior surface of each hole is plated with a conductive material.

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3 5. Structure as in Claim 4 wherein the conductive
4 material on the interior of each hole is electrically
5 connected to a corresponding one of said electrically
6 conductive traces.

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9 6. Structure as in Claim 1 including a multiplicity
10 of electronic components mounted on said printed circuit
11 board, each electrical lead of said electronic components
12 each making contact with a corresponding electrical contact
13 selected from said plurality of electrical contacts.

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7 7. Structure as in Claim 6 wherein said at least one
8 integrated circuit chip comprises one integrated circuit
9 chip.

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10 8. Structure as in Claim 1 wherein at least some of
11 said electrical contacts on said printed circuit board
12 comprise pads, each pad being connected to a corresponding
13 one of said plurality of electrically conductive traces
14 formed on said printed circuit board.

15 9. Structure as in Claim 8 wherein each pad is
16 connected by a conductive lead to a hole formed through said
17 printed circuit board, said hole being plated on its
18 interior surface by a conductive material and said hole
19 being in electrical contact with a corresponding one of said
20 electrically conductive traces formed on said printed
21 circuit board.

22 10. Structure as in Claim 1 wherein said printed
23 circuit board comprises:

24 a first portion thereof containing conductive
25 traces for interconnecting electronic components formed
26 thereon without the use of a programmable integrated
27 circuit; and

28 a second portion thereof containing at least one
29 programmable integrated circuit for interconnecting

1 electronic components formed on at least said second
2 portion of said printed circuit board.
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4 11. A printed circuit board comprising:
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6 a multiplicity of first electrical contacts formed
7 in said printed circuit board for receipt of the leads
8 of electronic components to be mounted on said printed
9 circuit board;

10 a corresponding multiplicity of second electrical
11 contacts formed in a selected region of said printed
12 circuit board for receipt of the leads on at least one
13 package of at least one integrated circuit chip to be
14 mounted on the printed circuit board for use in
15 interconnecting selected ones of said multiplicity of
16 first electrical contacts; and

17 conductive traces formed on said printed circuit
18 board, each conductive trace uniquely interconnecting
19 one first electrical contact to a corresponding second
20 electrical contact.

21 12. A printed circuit board as in Claim 11 including
22 at least one integrated circuit mounted thereon wherein said
23 at least one integrated circuit comprises a programmable
24 circuit for interconnecting selected conductive traces
25 formed on said printed circuit board thereby to form the
26 electronic components to be contained thereon into a
27 selected electrical circuit.

29 13. Structure as in Claim 12 including means for
30 testing the state of said at least one programmable
31 integrated circuit to determine the state of the signals on
32 said conductive traces.

34 14. Structure as in Claim 13 including means for
35 transmitting control signals to said at least one integrated
36 circuit for controlling the configuration of said at least
37 one integrated circuit so as to control the interconnection
38 of the conductive traces formed on said printed circuit

1 board.
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3 15. Structure as in Claim 14 including at least one
4 programmable integrated circuit mounted on said printed
5 circuit board for interconnecting selected traces formed on
6 said printed circuit board.
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8 16. Structure as in Claim 15 wherein said printed
9 circuit board comprises:

10 a first portion thereof containing conductive
11 traces for interconnecting electronic components formed
12 thereon without the use of a programmable integrated
13 circuit; and

14 a second portion thereof containing at least one
15 programmable integrated circuit for interconnecting
16 electronic components formed on at least said second
17 portion of said printed circuit board.

18 17. A printed circuit board comprising:

19 a multiplicity of component holes for receipt of
20 leads of electronic components;

21 a corresponding multiplicity of PIC holes for
22 receipt of the leads on the package or packages of a
23 programmable interconnect chip or chips; and

24 one or more layers of conductive traces formed on
25 said printed circuit board, each conductive trace
26 uniquely connecting one component hole to one PIC hole.
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28 18. Structure as in Claim 17 wherein said printed
29 circuit board comprises:

30 a first portion thereof containing conductive
31 traces for interconnecting electronic components formed
32 thereon without the use of a programmable integrated
33 circuit; and

34 a second portion thereof containing at least one
35 programmable integrated circuit for interconnecting
36 electronic components formed on at least said second
37 portion of said printed circuit board.
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1 19. The method of configuring an electronic system on
2 a printed circuit board comprising the steps of:
3 creating a computer model of the programmable PC
4 board containing a plurality of component contacts for
5 receipt of the leads of electronic components to be
6 mounted on said printed circuit board, a corresponding
7 plurality of PIC contacts for receipt of the leads of
8 one or more programmable interconnect chips ("PIC") for
9 use in interconnecting selected electronic components
10 and conductive traces, each conductive trace connecting
11 one component contact to one PIC contact;
12 simulating the placement and routing of select
13 electronic components on the component contacts;
14 simulating the electrical performance of the
15 system with the electrical components interconnected by
16 the PIC;
17 interconnecting the electronic components in a
18 desired fashion by configuring the PIC to achieve such
19 interconnection;
20 determining the system performance and system
21 characteristics with the electronic components so
22 interconnected by simulating and/or testing the system
23 so interconnected; and
24 repeating the above steps making those changes in
25 placement of electronic components as indicated to be
26 required by the simulation or test results until the
27 above steps yield an electronic system which yields the
28 desired characteristics and functional performance.

29 Subj A 6
30 20. A programmable interconnect chip for use in
31 interconnecting electronic components formed on a printed
32 circuit board, said chip comprising:
33 a first set of conductive leads formed in a first
34 direction across the surface of said chip, each of said
35 conductive leads comprising one or more conductive
36 segments, portions of selected ones of said segments
37 being connected to pads on the surface of said

1 programmable interconnect chip, each of said pads being
2 adapted for contact to a corresponding contact on the
3 printed circuit board;

4 a second set of conductors formed on said
5 programmable interconnect chip in a second direction
6 not parallel to said first direction, each conductive
7 lead in said second set of conductive leads comprising
8 one or more segments; and

9 means for electrically interconnecting selected
10 ones of said conductive leads in said first set of
11 conductive leads to one or more of said conductive
12 leads in said second set of conductive leads.

13 21. Structure as in Claim 20 wherein said programmable
14 interconnect chip comprises:

15 active transistor in said programmable
16 interconnect chip;

17 means for electrically connecting selected ones of
18 the segments of conductive leads in said first set of
19 conductive leads and in said second set of conductive
20 leads to programmable transistors in the substrate of
21 said programmable interconnect chip; and

22 means for programming said programmable
23 transistors in said interconnect chip so as to turn on
24 selected ones of the transistors in said programmable
25 interconnect chip to form desired interconnections
26 between selected contacts on said printed circuit
27 board.

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29 *E2* 22. Structure as in Claim 20 wherein said means for
30 electrically interconnecting comprise a plurality of
31 interconnect structures, each interconnect structure
32 comprising:

33 a first conductive layer comprising a portion of
34 the conductive segment of a conductive lead in said
35 first set of leads;

36 a second conductive layer comprising a portion of
37 the conductive segment of a conductive lead in said

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1 second set of conductive leads; and
2 dielectric formed between said first conductive
3 lead and said second conductive lead, said dielectric
4 being capable of being made conductive by the
5 application of a selected voltage thereto, thereby to
6 form an electrically conductive path from said
7 conductive segment in said first set of conductive
8 leads to said conductive segment in said second set of
9 conductive leads.

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